AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1	1. (Currently amended) A method for designing an integrated circuit
2	using a mask-programmable fabric, which contains both mask-programmable
3	logic and a mask-programmable interconnect, the method comprising:
4	receiving a description of a mask-programmable cell, wherein instances of
5	the mask-programmable cell are repeated to form the mask-programmable fabric;
6	wherein the description of the mask-programmable cell defines one
7	or more pins;
8	wherein a pin may be specified as being tied to, power, ground, a
9	route segment or another pin;
10	wherein a pin may be associated with a logic function; and
11	wherein a pin may be specified as part of a sequential element;
12	using the description of the mask-programmable cell to generate a derived
13	library containing cells that can be obtained by programming the mask-
14	programmable cell;
15	receiving a high-level design for the integrated circuit;
16	performing a synthesis operation on the high-level design to generate a
17	preliminary netlist for the high-level design that contains references to cells in the
18	derived library; and
19	converting the preliminary netlist into a netlist that contains references to
20	the mask-programmable cell.

1	2.	(Original) The method of claim 1, further comprising performing a
2	placement op	eration and a routing operation on the netlist to produce a layout for
3	the integrated	l circuit.
l	3.	(Original) The method of claim 2, wherein performing the routing

- operation involves programming the mask-programmable logic and mask-2 3 programmable interconnect.
- (Original) The method of claim 1, wherein the mask-1 4. 2 programmable logic and the mask-programmable interconnect that make up the 3 mask-programmable fabric can be programmed by changing inter-metal via layers 4 and/or metal layers
- 1 5. (Original) The method of claim 1, wherein the method further 2 comprises performing a packing operation on the netlist to combine cells that can use free resources from other cells. 3.
- 6. (Original) The method of claim 5, wherein performing the packing 1 2 operation involves considering: drive strengths of output pins for mask-programmable cells; 3 4 routability of pins for mask-programmable cells; 5 net count for mask-programmable cells; and 6 active pin count for mask-programmable cells.
- (Original) The method of claim 1, wherein the mask-7. 2 programmable cell includes a sequential logic portion, and wherein the derived 3 library contains a sequential cell, which corresponds the sequential logic portion of the mask-programmable cell. 4

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1	8. (Cancelled)
1	9. (Currently amended) The method of claim <u>81</u> ,
2	wherein the description of the mask-programmable cell defines route
3	segments for routing signals within the mask-programmable fabric;
4	wherein route segments may be horizontal, vertical or at any angle;
5	wherein several route segments may be collinear; and
6	wherein route segments may be coupled to pins or to other route segments.
1	10. (Original) The method of claim 9,
2	wherein the description of the mask-programmable fabric includes
3	information related to timing for route segments and connections; and
4	wherein the information related to timing can be used while performing a
5	routing operation for the mask-programmable fabric.
1	11. (Currently amended) A computer-readable storage medium storing
2	instructions that when executed by a computer cause the computer to perform a
3	method for designing an integrated circuit using a mask-programmable fabric,
4	which contains both mask-programmable logic and a mask-programmable
5	interconnect, the method comprising:
6	receiving a description of a mask-programmable cell, wherein instances of
7	the mask-programmable cell are repeated to form the mask-programmable fabric;
8	wherein the description of the mask-programmable cell defines one
9	or more pins;
10	wherein a pin may be specified as being tied to, power, ground, a
11	route segment or another pin;
12	wherein a pin may be associated with a logic function; and

13	wherein a pin may be specified as part of a sequential element;
14	using the description of the mask-programmable cell to generate a derived
15	library containing cells that can be obtained by programming the mask-
16	programmable cell;
17	receiving a high-level design for the integrated circuit;
18	performing a synthesis operation on the high-level design to generate a
19	preliminary netlist for the high-level design that contains references to cells in the
20	derived library; and
21	converting the preliminary netlist into a netlist that contains references to
22	the mask-programmable cell.
1	12. (Original) The computer-readable storage medium of claim 11,
2	wherein the method further comprises performing a placement operation and a
3	routing operation on the netlist to produce a layout for the integrated circuit.
1	13. (Original) The computer-readable storage medium of claim 12,
2	wherein performing the routing operation involves programming the mask-
3	programmable logic and mask programmable interconnect.
1	14. (Original) The computer-readable storage medium of claim 11,
2	wherein the mask-programmable logic and the mask-programmable interconnect
3	that make up the mask-programmable fabric can be programmed by changing
4	inter-metal via layers and/or metal layers.
1	15. (Original) The computer-readable storage medium of claim 11,
2	wherein the method further comprises performing a packing operation on the
3	netlist to combine cells that can use free resources from other cells.

l	16. (Original) The computer-readable storage medium of claim 15,
2	wherein performing the packing operation involves considering:
3	drive strengths of output pins for mask-programmable cells;
4	routability of pins for mask-programmable cells;
5	net count for mask-programmable cells; and
6	active pin count for mask-programmable cells.
1	17. (Original) The computer-readable storage medium of claim 11,
2	wherein the mask-programmable cell includes a sequential logic portion, and
3	wherein the derived library contains a sequential cell, which corresponds the
4	sequential logic portion of the mask-programmable cell.
1	18. (Cancelled)
1	19. (Currently amended) The computer-readable storage medium of
2	claim 18 <u>11</u> ,
3	wherein the description of the mask-programmable cell defines route
4	segments for routing signals within the mask-programmable fabric;
5	wherein route segments may be horizontal, vertical or at any angle;
6	wherein several route segments may be collinear; and
7	wherein route segments may be coupled to pins or to other route segments
1	20. (Original) The computer-readable storage medium of claim 19,
2	wherein the description of the mask-programmable fabric includes
3	information related to timing for route segments and connections; and
4	wherein the information related to timing can be used while performing a
5	routing operation for the mask-programmable fabric.

1	21. (Currently amended) An apparatus that facilitates designing an
2	integrated circuit using a mask-programmable fabric, which contains both mask-
3	programmable logic and a mask-programmable interconnect, the apparatus
4	comprising:
5	a receiving mechanism configured to receive a description of a mask-
6	programmable cell, wherein instances of the mask-programmable cell are repeated
7	to form the mask-programmable fabric;
8	wherein the description of the mask-programmable cell defines one
9	or more pins;
10	wherein a pin may be specified as being tied to, power, ground, a
11	route segment or another pin;
12	wherein a pin may be associated with a logic function; and
13	wherein a pin may be specified as part of a sequential element;
14	a deriving mechanism configured to use the description of the mask-
15	programmable cell to generate a derived library containing cells that can be
16	obtained by programming the mask-programmable cell;
17	wherein the receiving mechanism is additionally configured to receive a
18	high-level design for the integrated circuit;
19	a synthesis mechanism configured to perform a synthesis operation on the
20	high-level design to generate a preliminary netlist for the high-level design that
21	contains references to cells in the derived library; and
22	a conversion mechanism configured to convert the preliminary netlist into
23	a netlist that contains references to the mask-programmable cell.
1	22. (Original) The apparatus of claim 21, further comprising a
2	placement mechanism and a routing mechanism configured to perform a
3	placement operation and a routing operation, respectively, on the netlist to
4	produce a layout for the integrated circuit.

1	23.	(Original) The apparatus of claim 22, wherein the routing
2	mechanism is	configured to program the mask-programmable logic and mask
3	programmable	e interconnect.
1	24.	(Original) The apparatus of claim 21, wherein the mask-
2	programmable	e logic and the mask-programmable interconnect that make up the
3	mask-progran	nmable fabric can programmed by changing inter-metal via layers
4	and/or metal l	ayers.
1	25.	(Original) The apparatus of claim 21, wherein the apparatus further
2	comprises a p	acking mechanism configured to perform a packing operation on the
3	netlist to com	bine cells that can use free resources from other cells.
1	26.	(Original) The apparatus of claim 25, wherein performing the
2	packing opera	ation involves considering:
3	drive	strengths of output pins for mask-programmable cells;
4	routab	pility of pins for mask-programmable cells;
5	net co	unt for mask-programmable cells; and
6	active	pin count for mask-programmable cells.
1	27.	(Original) The apparatus of claim 21, wherein the mask-
2	programmabl	e cell includes a sequential logic portion, and wherein the derived
3	library contai	ns a sequential cell, which corresponds the sequential logic portion
4	of the mask-p	rogrammable cell.
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(Cancelled)

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1	29. (Currently amended) The apparatus of claim 2821,
2	wherein the description of the mask-programmable cell defines route
3	segments for routing signals within the mask-programmable fabric;
4	wherein route segments may be horizontal, vertical or at any angle;
5	wherein several route segments may be collinear; and
6	wherein route segments may be coupled to pins or to other route segments.
1	30. (Original) The apparatus of claim 29,
2	wherein the description of the mask-programmable fabric includes
3	information related to timing for route segments and connections; and
4	wherein the information related to timing can be used while performing a
5	routing operation for the mask-programmable fabric.
1	31. (Currently amended) An integrated circuit created through a
2	process that uses a mask-programmable fabric to design the integrated circuit,
3	wherein the mask-programmable fabric contains both mask-programmable logic
4	and a mask-programmable interconnect, the process comprising:
5	receiving a description of a mask-programmable cell, wherein instances of
6	the mask-programmable cell are repeated to form the mask-programmable fabric;
7	wherein the description of the mask-programmable cell defines one
8	or more pins;
9	wherein a pin may be specified as being tied to, power, ground, a
10	route segment or another pin;
11	wherein a pin may be associated with a logic function; and
12	wherein a pin may be specified as part of a sequential element;

13	using the description of the mask-programmable cell to generate a derived	
14	library containing cells that can be obtained by programming the mask-	
15	programmable cell;	
16	receiving a high-level design for the integrated circuit;	
17	performing a synthesis operation on the high-level design to generate a	
18	preliminary netlist for the high-level design that contains references to cells in the	
19	derived library; and	
20	converting the preliminary netlist into a netlist that contains references to	
21	the mask-programmable cell.	
1	32. (Currently amended) A mask for use in an optical lithography	
2	process for manufacturing an integrated circuit, wherein the mask is generated	
3	through a process that uses a mask-programmable fabric to design the integrated	
4	circuit, wherein the mask-programmable fabric contains both mask-programmable	
5	logic and a mask-programmable interconnect, the process comprising:	
6	receiving a description of a mask-programmable cell, wherein instances of the	
7	mask-programmable cell are repeated to form the mask-programmable fabric;	
8	wherein the description of the mask-programmable cell defines on	
9	or more pins;	
10	wherein a pin may be specified as being tied to, power, ground, a	
11	route segment or another pin;	
12	wherein a pin may be associated with a logic function; and	
13	wherein a pin may be specified as part of a sequential element;	
14	using the description of the mask-programmable cell to generate a derived	
15	library containing cells that can be obtained by programming the mask-	
16	programmable cell;	
17	receiving a high-level design for the integrated circuit	

performing a synthesis operation on the high-level design to generate a
preliminary netlist for the high-level design that contains references to cells in the
derived library; and
converting the preliminary netlist into a netlist that contains references to
the mask-programmable cell.